CLAIMS

1. A method of forming a memory circuit comprising a plurality of six transistor memory cells, comprising the steps for each of the six transistor memory cells of:

forming a first inverter having an input and an output, and comprising:

a first transistor forming a first drive transistor comprising first and second source/drain regions and a gate;

a second transistor forming a first pull-up transistor comprising first and second source/drain regions and a gate;

wherein the output of the first inverter is coupled to the first source/drain region of the first drive transistor and to the first source/drain region of the first pull up transistor;

forming a second inverter having an input and an output, and comprising:

a third transistor forming a second drive transistor comprising first and second source/drain regions and a gate;

a fourth transistor forming a second pull-up transistor comprising first and second source/drain regions and a gate;

wherein the output of the second inverter is coupled to the second source/drain region of the second drive transistor and to the first source/drain region of the second pull up transistor;

forming a fifth transistor forming a first access transistor having a gate and having a first source/drain region coupled to the output of the first inverter and a second source/drain region for communicating to a first bit line;

forming a sixth transistor forming a second access transistor having a gate and having a first source/drain region coupled to the output of the second inverter and a second source/drain region for communicating to a second bit line;

forming at least one insulating layer in a position relative to the first through sixth transistors;

applying a first mask to the at least one insulating layer to form a plurality of vias through the at least one insulating layer;

forming a first conducting layer comprising a plurality of conducting plugs in the plurality of vias, wherein the plurality of conducting plugs comprise:

a first conducting plug coupled to the first source/drain region of the first drive transistor;

a second conducting plug coupled to the first source/drain region of the first pull-up transistor and to the gate of the second drive transistor and to the gate of the second pull-up transistor;

a third conducting plug coupled to the first source/drain region of the second drive transistor; and

a fourth conducting plug coupled to the first source/drain region of the second pull-up transistor and to the gate of the first drive transistor and to the gate of the first pull-up transistor;

forming a second conducting layer comprising a plurality of conducting elements, wherein the plurality of conducting elements comprise:

a first conducting element coupled to and physically contacting the first conducting plug and coupled to and physically contacting the second conducting plug; and

a second conducting element coupled to and physically contacting the third conducting plug and coupled to and physically contacting the fourth conducting plug.

2. The method of claim 1 wherein the step of forming a second conducting layer comprising a plurality of conducting elements comprises applying a next successive mask after the first mask.

3. The method of claim 2 and further comprising applying a surface treatment to the at least one insulating layer and the first conducting layer prior to the step of forming the second conducting layer.

4. The method of claim 2:

wherein each of the plurality of conducting plugs comprises a lower surface, an upper surface generally parallel to the lower surface, and one or more heights at respective vertical positions between the lower surface and the upper surface; and

wherein the step of forming a second conducting layer comprises forming a second layer which is parallel to the substrate and having a lower surface extending primarily parallel to the substrate and defining an imaginary ~~line~~ plane SM 8/9/00 along the lower surface and primarily parallel to the substrate, and wherein at each reference point proximate a corresponding one of the conducting plugs a vertical distance from the imaginary ~~line~~ plane SM 8/9/00 to a lower surface of the corresponding conducting plug is no greater than the height at the corresponding vertical position.

5. The method of claim 4, wherein for each of the six transistor memory cells the cell further comprises:

a first continuous active region strip, comprising:

the first and second source/drain regions of the first transistor forming a first drive transistor; and

the first and second source/drain regions of the fifth transistor forming a first access transistor; and

a second continuous active region strip, comprising:

the first and second source/drain regions of the third transistor forming a second drive transistor; and

the first and second source/drain regions of the sixth transistor forming a second access transistor.

6. The method of claim 5, wherein each of the first and second continuous active region strips comprise a first conductivity type, and wherein for each of the six transistor memory cells the cell further comprises:

a third continuous active region strip of a second conductivity type differing from the first conductivity type, and comprising the first and second source/drain regions of the second transistor forming a first pull-up transistor; and

a fourth continuous active region strip of the second conductivity type and comprising the first and second source/drain regions of the fourth transistor forming a second pull-up transistor.

7. The method of claim 6, wherein for each of the six transistor memory cells the first, second, third, and fourth continuous active region strips are aligned in a same dimension.

8. The method of claim 7, wherein for each of the six transistor memory cells the cell further comprises:

a first conductor structure comprising the gate of the first transistor forming a first drive transistor and the gate of the second transistor forming a first pull-up transistor; and

a second conductor structure comprising the gate of the third transistor forming a second drive transistor and the gate of the fourth transistor forming a second pull-up transistor.

9. The method of claim 8, wherein the same dimension comprises a first same dimension, and wherein for each of the six transistor memory cells the first and second conductor structures are aligned in a second same dimension that is generally perpendicular to the first same dimension.

10. The method of claim 9, wherein for each of the six transistor memory cells the cell further comprises:

a third conductor structure comprising the gate of the fifth transistor forming a first access transistor; and

a fourth conductor structure comprising the gate of the sixth transistor forming a second access transistor.

11. The method of claim 10 wherein for each of the six transistor memory cells the third and fourth conductor structures are aligned in the second same dimension.

12. The method of claim 11, wherein for each of the six transistor memory cells, the first conducting layer comprises tungsten and the second conducting layer comprises aluminum.

13. The method of claim 11, wherein for each of the six transistor memory cells, the first conducting layer comprises tungsten and the second conducting layer comprises copper.

14. The method of claim 11, wherein for each of the six transistor memory cells, the first conducting layer comprises at least one material selected from the group consisting of titanium, titanium nitride, tungsten aluminum and copper.

15. The method of claim 11, wherein for each of the six transistor memory cells, the second conducting layer comprises at least one material selected from the group consisting of titanium, titanium nitride, tungsten aluminum and copper.

16. The method of claim 11, wherein for each of the six transistor memory cells:

the first conducting layer comprises at least one material selected from the group consisting of titanium, titanium nitride, tungsten aluminum and copper; and

the second conducting layer comprises at least one material selected from the group consisting of titanium, titanium nitride, tungsten aluminum and copper.

17. The method of claim 1:

wherein each of the plurality of conducting plugs comprises a lower surface proximate and parallel to a substrate, an upper surface parallel to the lower surface, and a height between the lower surface and the upper surface; and

wherein the step of forming a second conducting layer comprises forming a second layer parallel to the substrate and having a lower surface extending primarily parallel to the substrate, and wherein a distance from the lower surface of the second layer to the lower surface of the plurality of conducting plugs is no greater than the first height.

18. The method of claim 1, wherein for each of the six transistor memory cells the cell further comprises:

a first continuous active region strip, comprising:

the first and second source/drain regions of the first transistor forming a first drive transistor; and

the first and second source/drain regions of the fifth transistor forming a first access transistor; and

a second continuous active region strip, comprising:

the first and second source/drain regions of the third transistor forming a second drive transistor; and

the first and second source/drain regions of the sixth transistor forming a second access transistor.

19. The method of claim 18, wherein each of the first and second continuous active region strips comprise a first conductivity type, and wherein for each of the six transistor memory cells the cell further comprises:

a third continuous active region strip of a second conductivity type differing from the first conductivity type, and comprising the first and second source/drain regions of the second transistor forming a first pull-up transistor; and

a fourth continuous active region strip of the second conductivity type and comprising the first and second source/drain regions of the fourth transistor forming a second pull-up transistor.

20. The method of claim 19, wherein for each of the six transistor memory cells the first, second, third, and fourth continuous active region strips are aligned in a same dimension.

21. The method of claim 20, wherein for each of the six transistor memory cells the cell further comprises:

a first conductor structure comprising the gate of the first transistor forming a first drive transistor and the gate of the second transistor forming a first pull-up transistor; and

a second conductor structure comprising the gate of the third transistor forming a second drive transistor and the gate of the fourth transistor forming a second pull-up transistor.

22. The method of claim 21, wherein the same dimension comprises a first same dimension, and wherein for each of the six transistor memory cells the first and second conductor structures are aligned in a second same dimension that is generally perpendicular to the first same dimension.

23. The method of claim 22, wherein for each of the six transistor memory cells the cell further comprises:

a third conductor structure comprising the gate of the fifth transistor forming a first access transistor; and

a fourth conductor structure comprising the gate of the sixth transistor forming a second access transistor.

24. The method of claim 23 wherein for each of the six transistor memory cells the third and fourth conductor structures are aligned in the second same dimension.

25. The method of claim 24, wherein for each of the six transistor memory cells, the first conducting layer comprises tungsten and the second conducting layer comprises copper.

26. The method of claim 1 wherein for each of the six transistor memory cells:

the first conducting layer and the gates of each of the first through the sixth transistors share a common first plane; and

the second conducting layer is located at a plane different than the common first plane.

27. The method of claim 26:

wherein the second conducting plug has a length and a width;

wherein the length of the second conducting plug is greater than the width of the second conducting plug;

wherein the length of the second conducting plug is primarily perpendicular to the gate of the first drive transistor and to the gate of the first pull-up transistor;

wherein the fourth conducting plug has a length and a width;

wherein the length of the fourth conducting plug is greater than the width of the fourth conducting plug; and

wherein the length of the fourth conducting plug is primarily perpendicular to the gate of the second drive transistor and to the gate of the second pull-up transistor.

28. The method of claim 27:

wherein the length of the second conducting plug is greater than 1.5 times the width of the second conducting plug; and

wherein the length of the fourth conducting plug is greater than 1.5 times the width of the fourth conducting plug.

29. The method of claim 2:

wherein the second conducting plug has a length and a width;

wherein the length of the second conducting plug is greater than the width of the second conducting plug;

wherein the length of the second conducting plug is primarily perpendicular to the gate of the first drive transistor and to the gate of the first pull-up transistor;

wherein the fourth conducting plug has a length and a width;

wherein the length of the fourth conducting plug is greater than the width of the fourth conducting plug; and

wherein the length of the fourth conducting plug is primarily perpendicular to the gate of the second drive transistor and to the gate of the second pull-up transistor.

30. The method of claim 29:

wherein the length of the second conducting plug is greater than 1.5 times the width of the second conducting plug; and

wherein the length of the fourth conducting plug is greater than 1.5 times the width of the fourth conducting plug.

31. A method of forming a memory circuit comprising a plurality of six transistor memory cells, comprising the steps for each of the six transistor memory cells of:

forming a first inverter having an input and an output, and comprising:

a first transistor forming a first drive transistor comprising first and second source/drain regions and a gate;

a second transistor forming a first pull-up transistor comprising first and second source/drain regions and a gate;

wherein the output of the first inverter is coupled to the first source/drain region of the first drive transistor and to the first source/drain region of the first pull up transistor;

forming a second inverter having an input and an output, and comprising:

a third transistor forming a second drive transistor comprising first and second source/drain regions and a gate;

a fourth transistor forming a second pull-up transistor comprising first and second source/drain regions and a gate;

wherein the output of the second inverter is coupled to the first source/drain region of the second drive transistor and to the first source/drain region of the second pull up transistor;

forming a fifth transistor forming a first access transistor having a gate and having a first source/drain region coupled to the output of the first inverter and a second source/drain region for communicating to a first bit line;

forming a sixth transistor forming a second access transistor having a gate and having a first source/drain region coupled to the output of the second inverter and a second source/drain region for communicating to a second bit line;

forming at least one insulating layer in a position relative to the first through sixth transistors;

applying a first mask to the at least one insulating layer to form a plurality of vias through the at least one insulating layer;

forming a first conducting layer comprising a plurality of conducting plugs in the plurality of vias, wherein the plurality of conducting plugs comprise:

a first set of conducting plugs, wherein each plug in the first set is coupled to any one of either any of the source/drain regions or the gate of any of the first through sixth transistors;

a second set of conducting plugs, wherein each plug in the second set is coupled to more than one of either any of the source/drain regions or the gate of any of the first through sixth transistors;

forming a second conducting layer comprising a plurality of conducting elements, wherein the plurality of conducting elements comprise:

a first set of conducting elements, wherein each element in the first set of conducting elements is coupled to only one conducting plug in the first set of conducting plugs; and

a second set of conducting elements, wherein each element in the second set of conducting elements is coupled between a conducting plug in the first set of conducting plugs and a conducting plug in the second set of conducting plugs.

32. The method of claim 31 wherein the step of forming a second conducting layer comprising a plurality of conducting elements comprises applying a next successive mask after the first mask.

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33. A memory circuit comprising a plurality of six transistor memory cells, wherein each of the six transistor memory cells comprises:

a first inverter having an input and an output, and comprising:

a first transistor forming a first drive transistor comprising first and second source/drain regions and a gate;

a second transistor forming a first pull-up transistor comprising first and second source/drain regions and a gate;

wherein the output of the first inverter is coupled the first source/drain region of the first drive transistor and to the first source/drain region of the first pull up transistor;

a second inverter having an input and an output, and comprising:

a third transistor forming a second drive transistor comprising first and second source/drain regions and a gate;

a fourth transistor forming a second pull-up transistor comprising first and second source/drain regions and a gate;

wherein the output of the second inverter is coupled to the first source/drain region of the second drive transistor and to the first source/drain region of the second pull up transistor;

a fifth transistor forming a first access transistor having a gate and having a first source/drain region coupled to the output of the first inverter and a second source/drain region for communicating to a first bit line;

a sixth transistor forming a second access transistor having a gate and having a first source/drain region coupled to the output of the second inverter and a second source/drain region for communicating to a second bit line;

at least one insulating layer in a position relative to the first through sixth transistors;

forming a first conducting layer comprising a plurality of conducting plugs formed in a plurality of vias in the at least one insulating layer, wherein the plurality of conducting plugs comprise:

a first conducting plug coupled to the first source drain of the first drive transistor;

a second conducting plug coupled to the first source/drain region of the first pull-up transistor and to the gate of the second drive transistor and to the gate of the second pull-up transistor;

a third conducting plug coupled to the first source/drain region of the second drive transistor; and

a fourth conducting plug coupled to the first source/drain region of the second pull-up transistor and to the gate of the first drive transistor and to the gate of the first pull-up transistor;

a second conducting layer comprising a plurality of conducting elements, wherein the plurality of conducting elements comprise:

a first conducting element coupled to and physically contacting the first conducting plug and coupled to and physically contacting the second conducting plug; and

a second conducting element coupled to and physically contacting the third conducting plug and coupled to and physically contacting the fourth conducting plug.

34. The memory circuit of claim 33:

wherein each of the plurality of conducting plugs comprises a lower surface, an upper surface generally parallel to the lower surface, and one or more heights at respective vertical positions between the lower surface and the upper surface; and

wherein the step of forming a second conducting layer comprises forming a second layer which is parallel to the substrate and having a lower surface extending primarily parallel to the substrate, and wherein the lower surface of the second layer at each reference point proximate a corresponding one of the conducting plugs is at a vertical distance from the lower surface of the corresponding conducting plug that is no greater than the height at the corresponding vertical position.

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